

EXHIBIT R

(12) **United States Patent**
Ichiyoshi

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(54) **TEST APPARATUS AND TEST METHOD
FOR TESTING PLURALITY OF DEVICES IN
PARALLEL**

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G01R 31/3185 (2006.01)

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714/718

(58) **Field of Classification Search** 714/742,
714/738, 736, 724, 718, 5, 25, 42, 54, 715
See application file for complete search history.

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Primary Examiner—Cynthia Britt

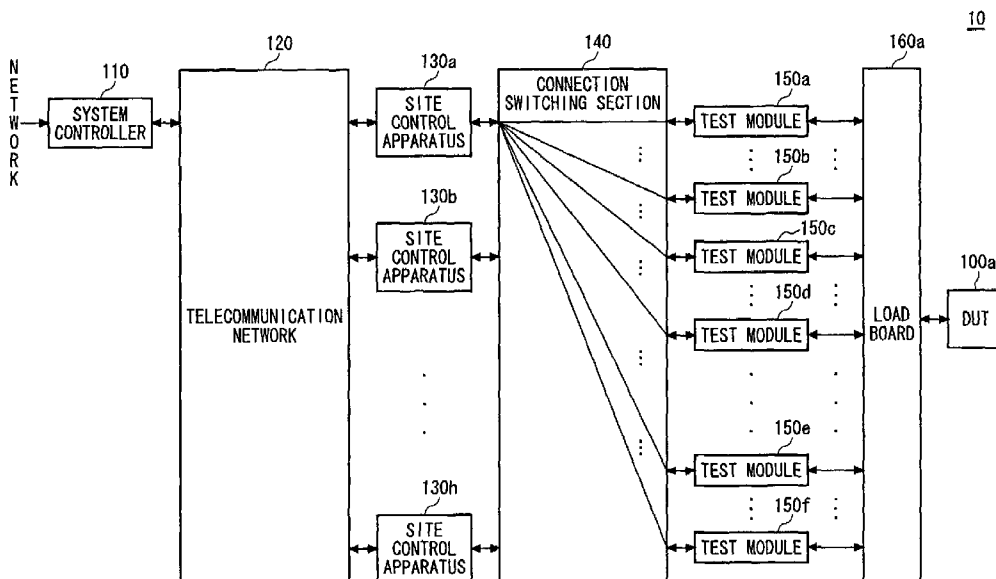
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(57) **ABSTRACT**

A test apparatus according to the present invention includes: a plurality of test modules, connected to either of the plurality of devices under test, for supplying a test signal to the connected device under test; a plurality of control apparatuses for controlling the plurality of test modules, and for testing the plurality of devices under test in parallel; and a connection switching section for switching topology of the plurality of control apparatuses and the plurality of test modules so that the plurality of control apparatuses connect with the plurality of devices under test respectively.

8 Claims, 14 Drawing Sheets



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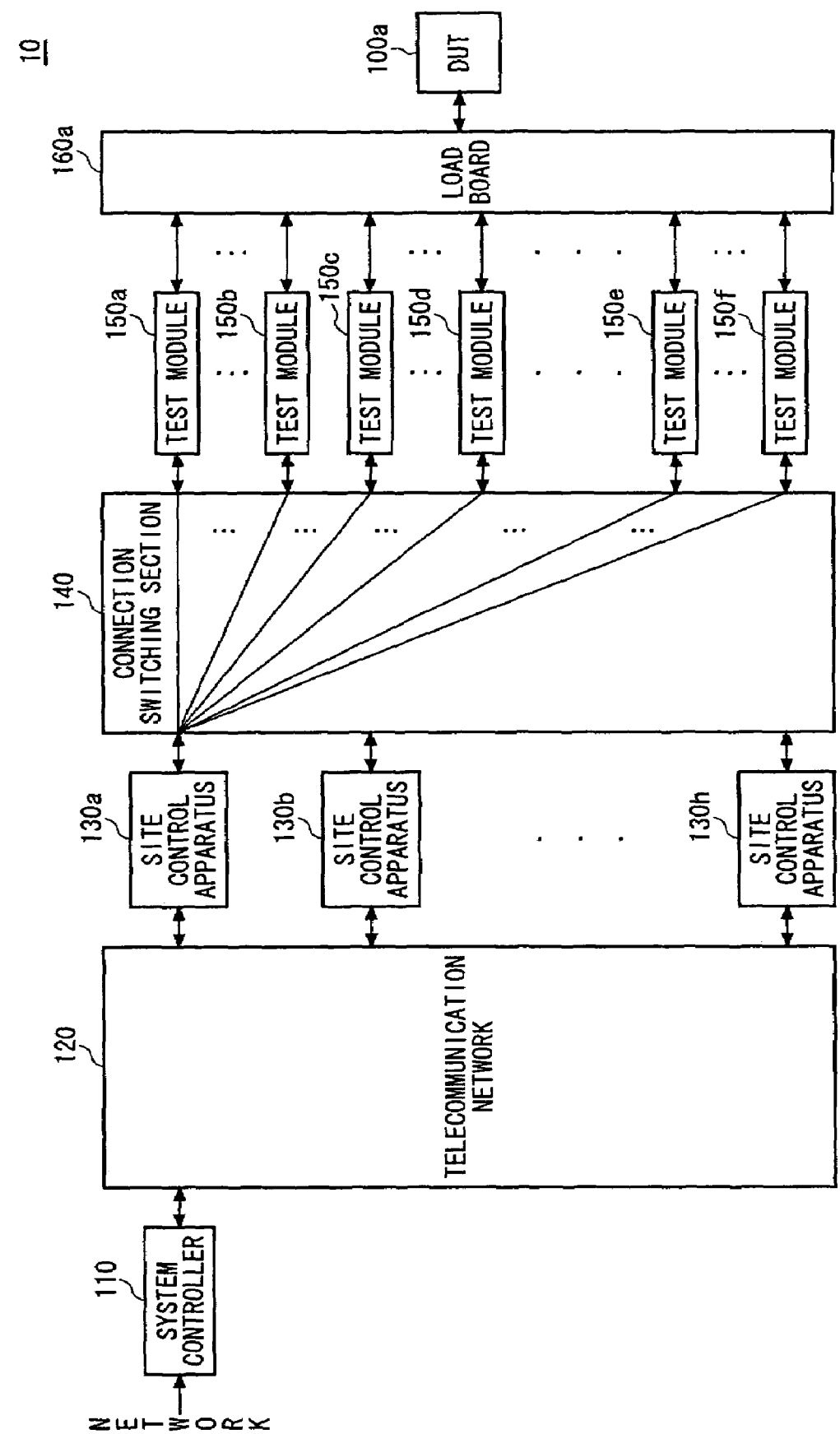


FIG. 1

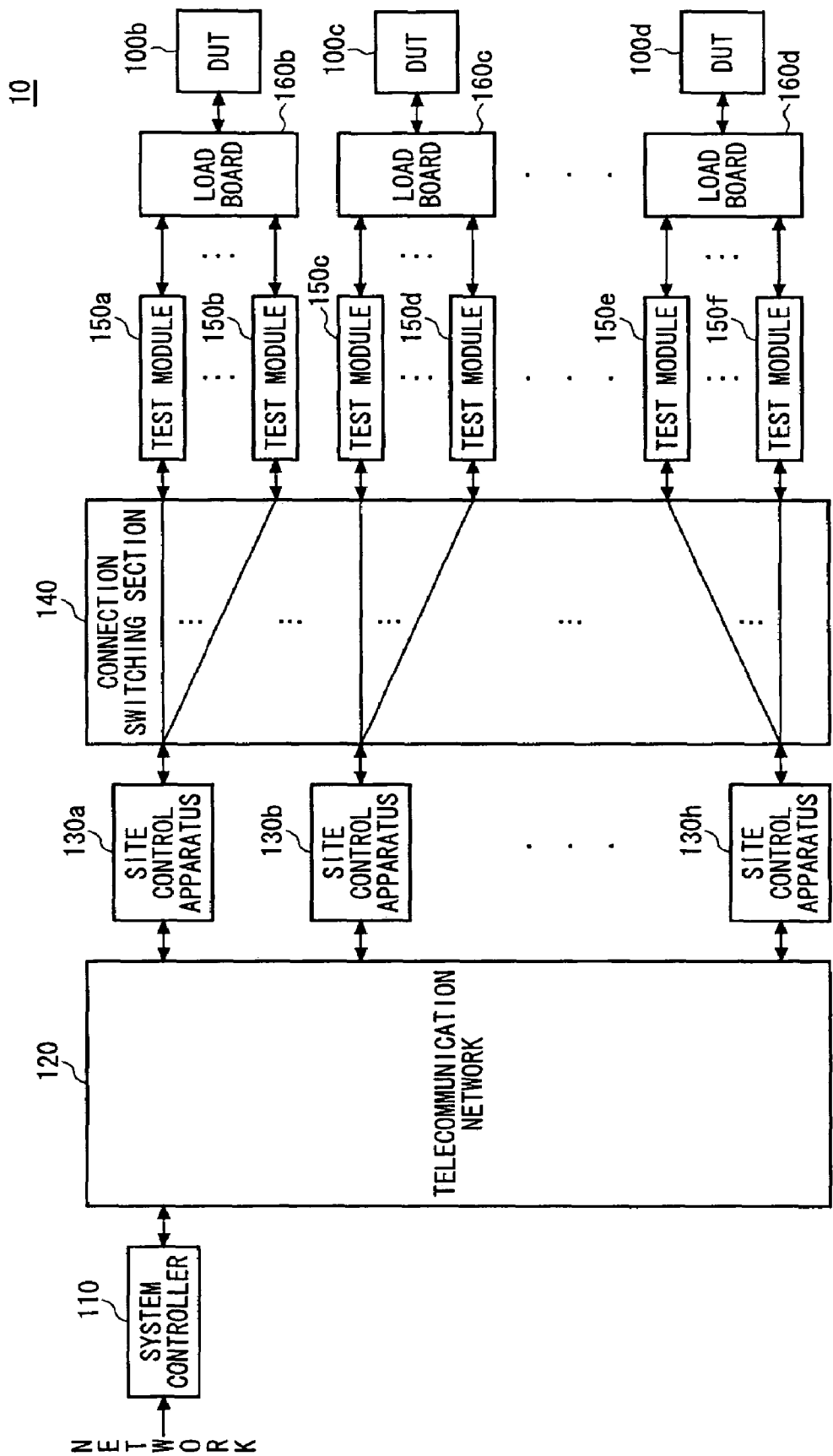


FIG. 2

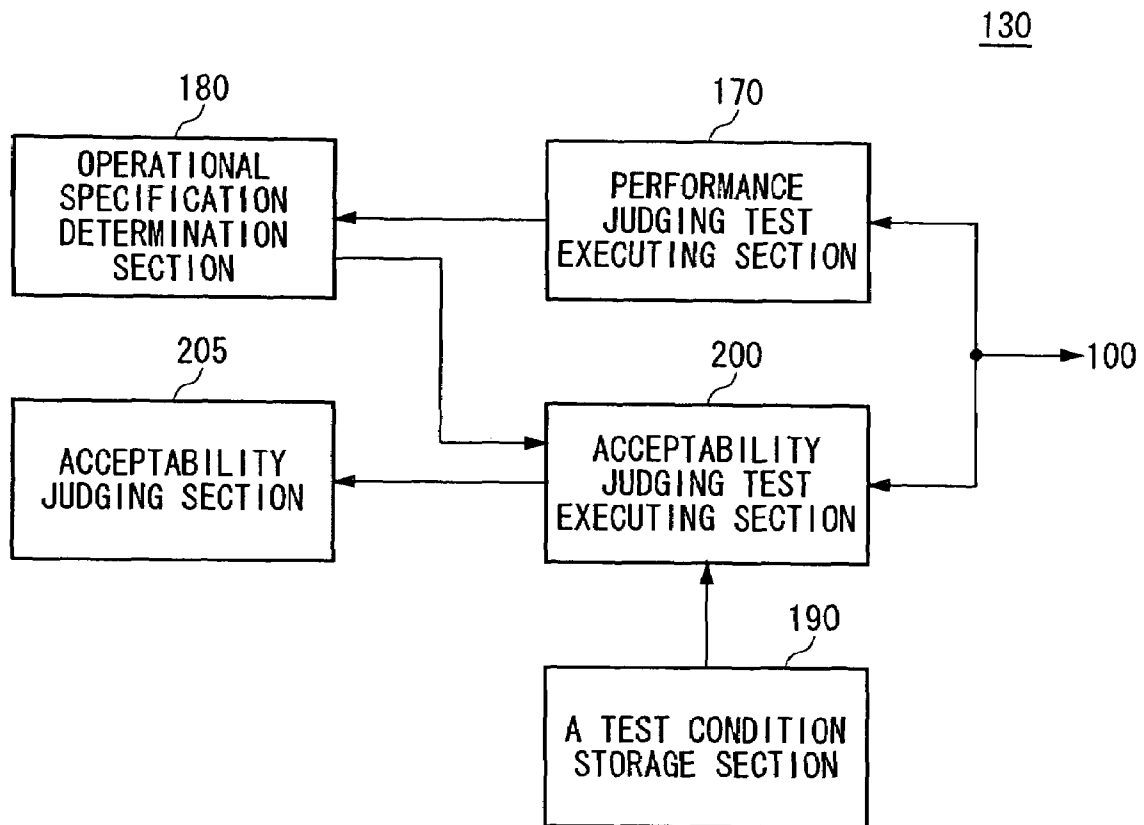


FIG. 3

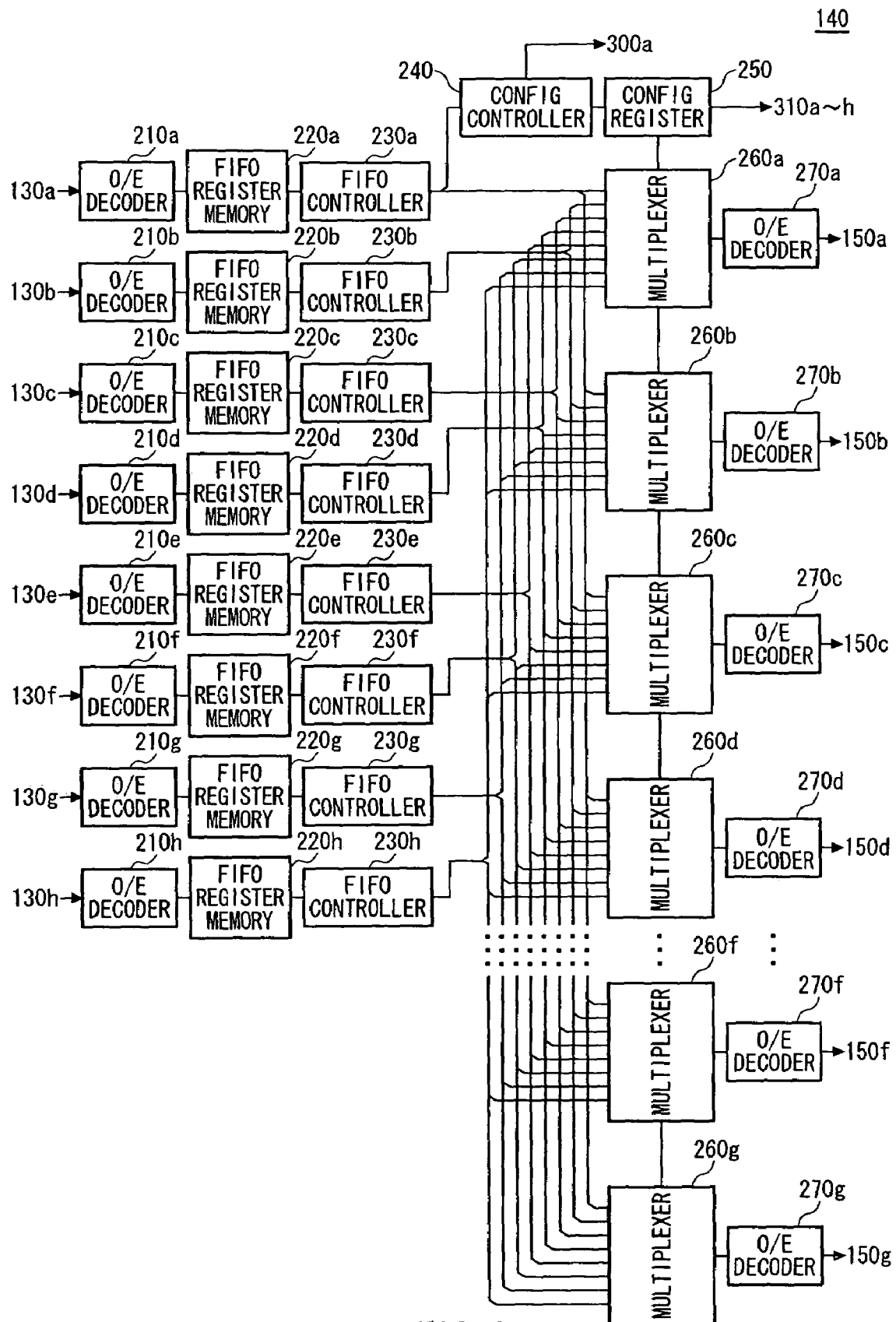


FIG. 4

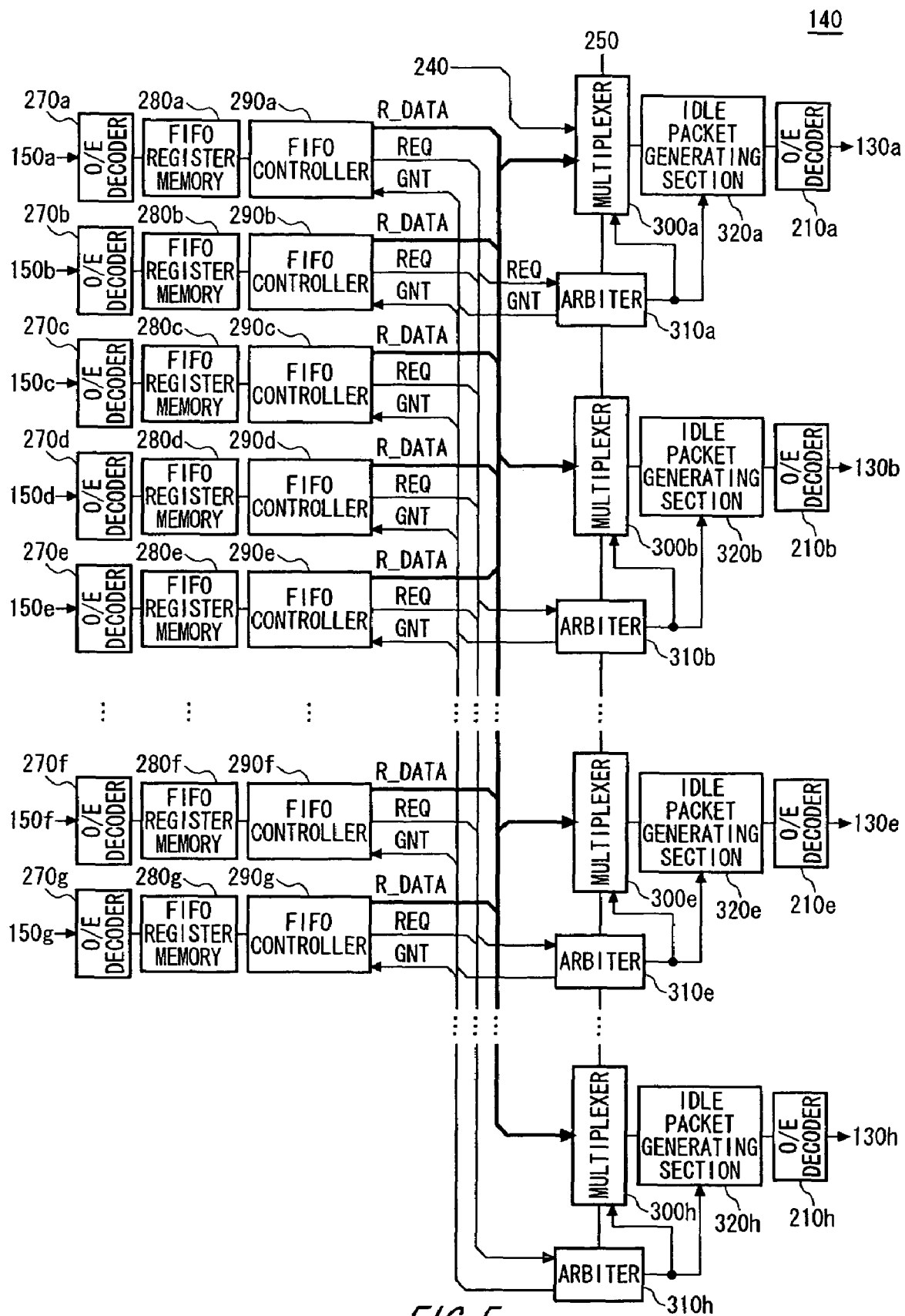


FIG. 5

250

⋮	⋮	300
17h	Switch Select 1	
18h	Switch Select 2	
19h	Switch Select 3	
1Ah	Switch Select 4	
1Bh	Switch Select 5	
1Ch	Switch Select 6	
1Dh	Switch Select 7	
1Eh	Switch Select 8	
⋮	⋮	

FIG. 6

300

Port 8		Port 7		Port 6		Port 5		Port 4		Port 3		Port 2		Port 1	
ON	CPU No.	ON	CPU No.	ON	CPU No.	ON	CPU No.	ON	CPU No.	ON	CPU No.	ON	CPU No.	ON	CPU No.

FIG. 7

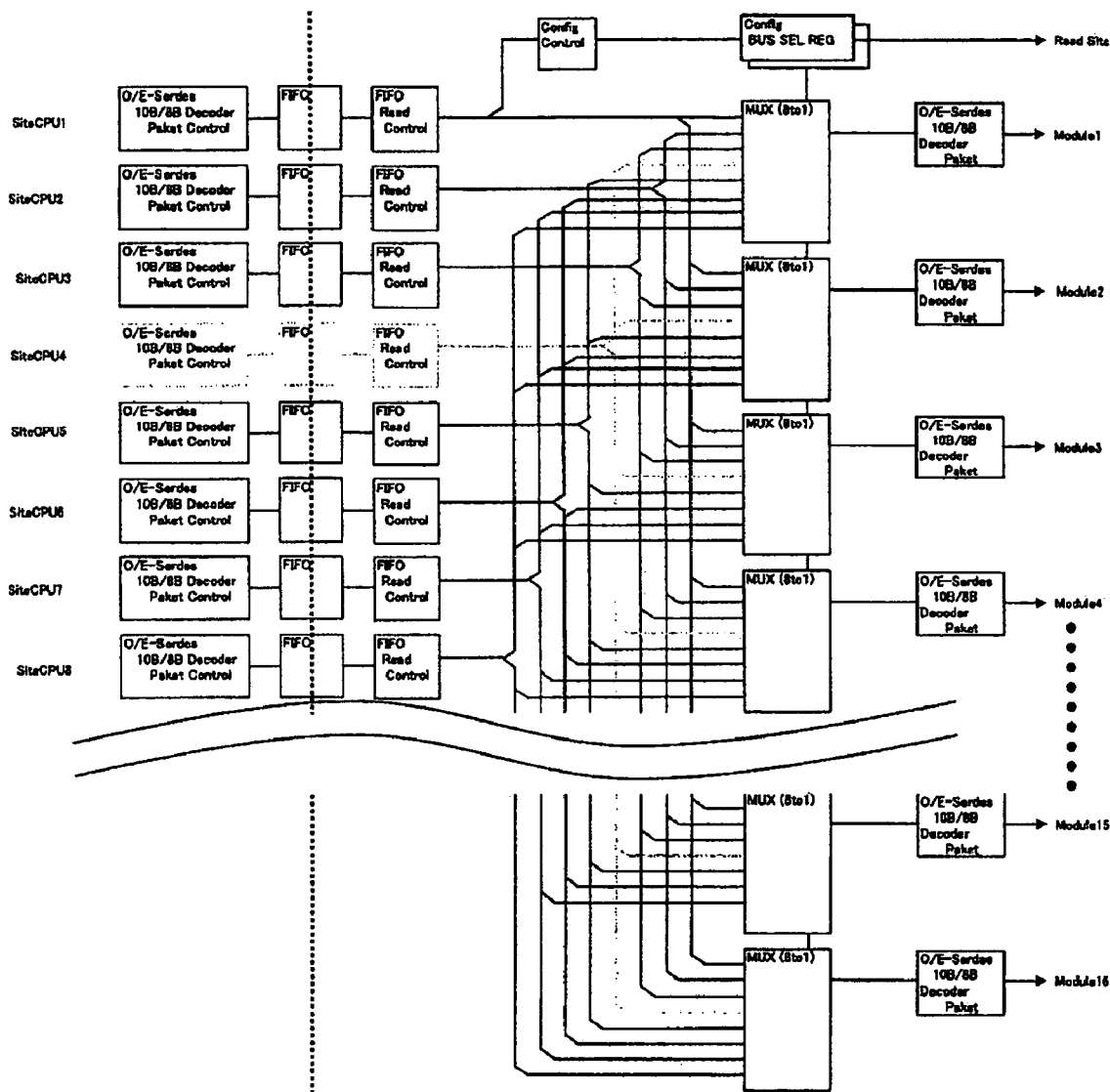


FIG. 8

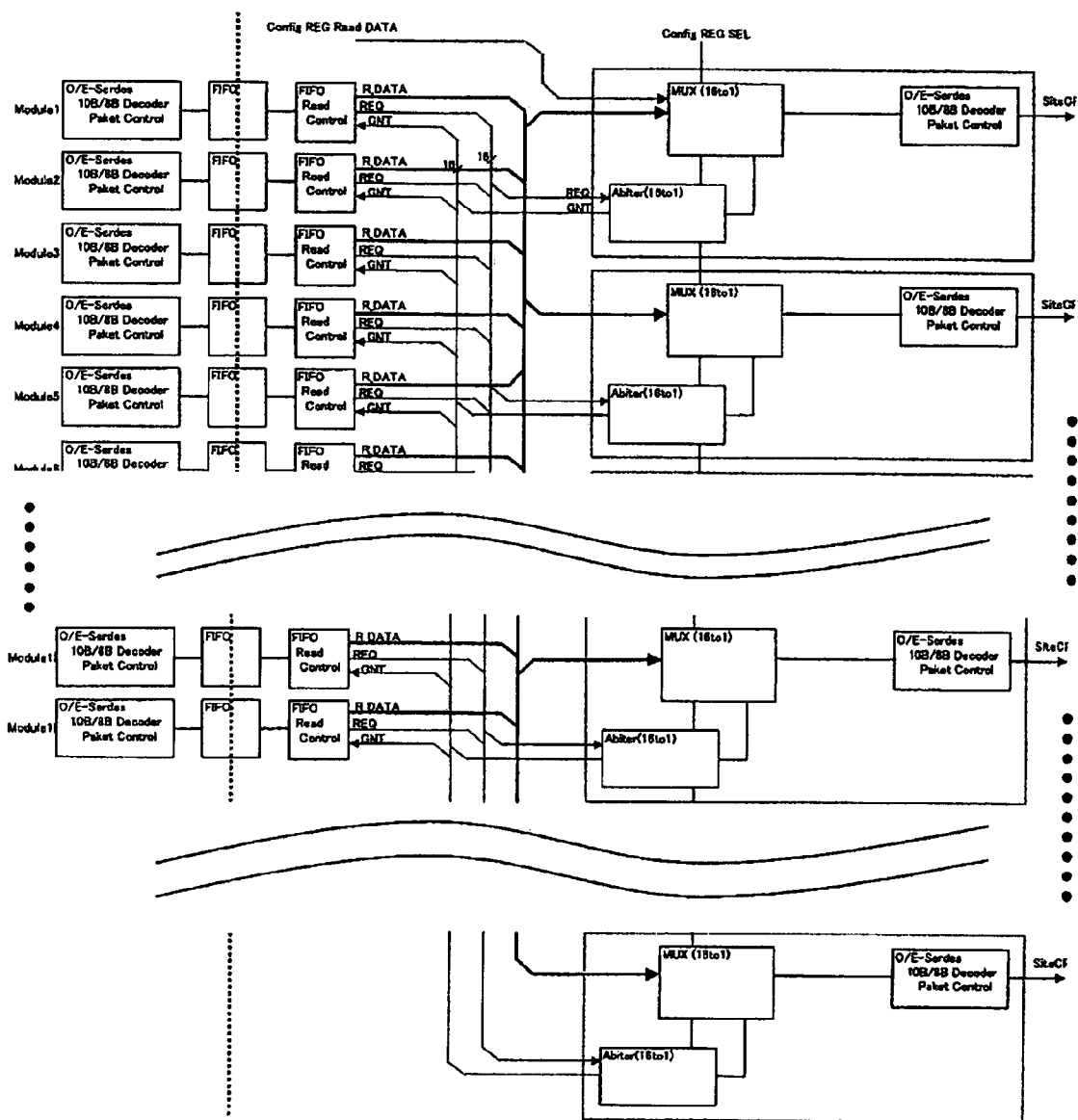


FIG. 9

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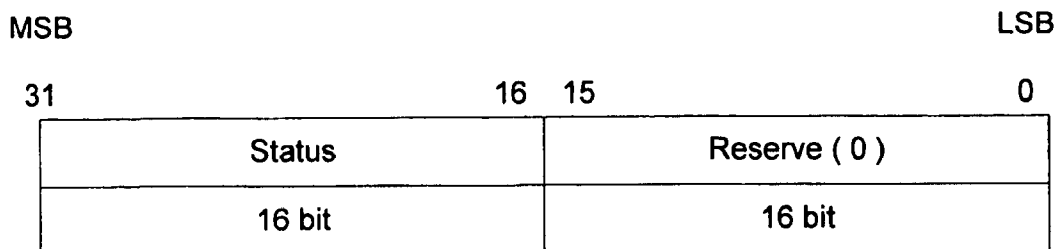
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FIG. 10

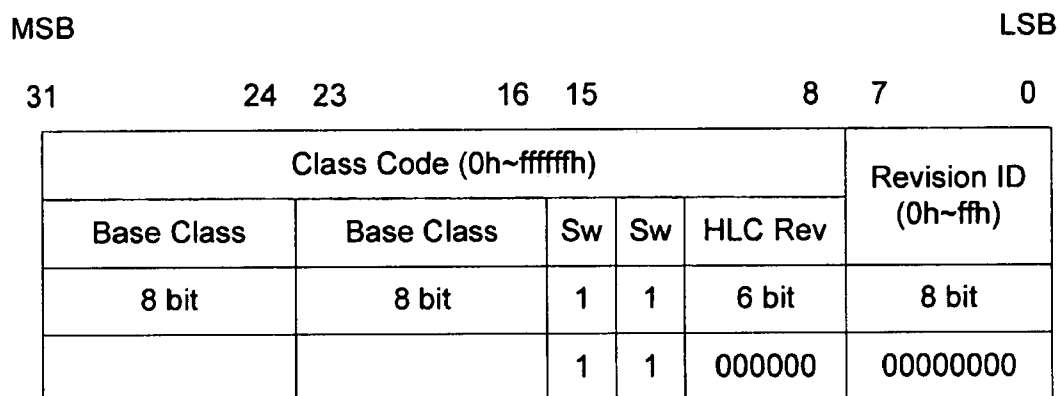


FIG. 11

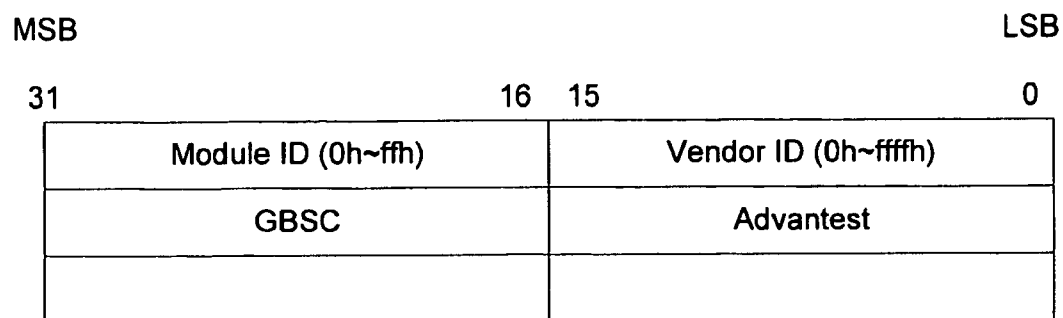


FIG. 12

FIG. 14

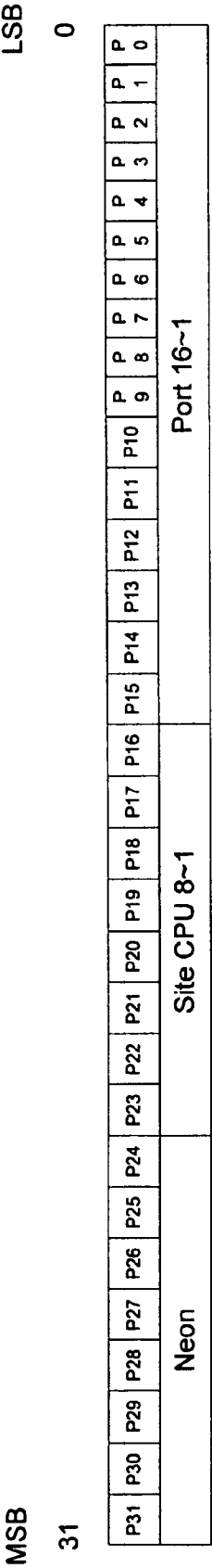


FIG. 15

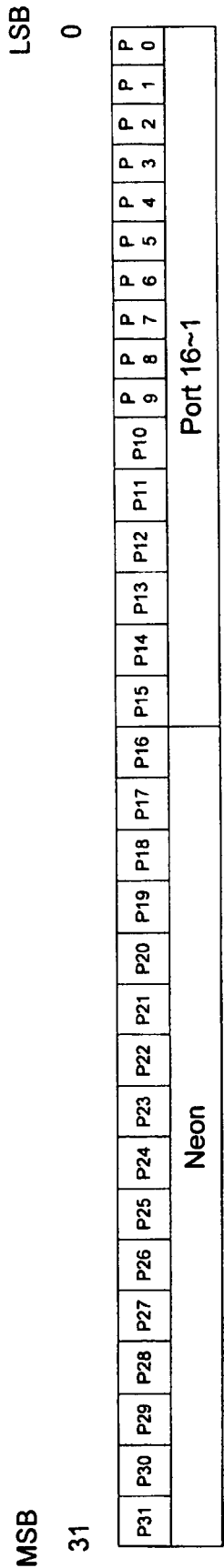


FIG. 16

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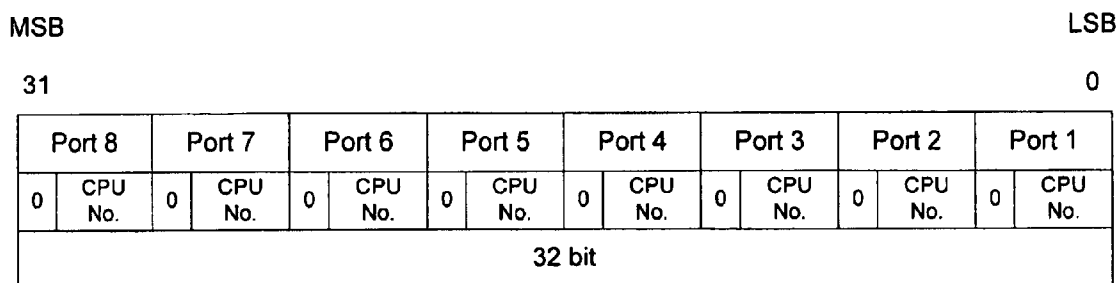
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FIG. 17

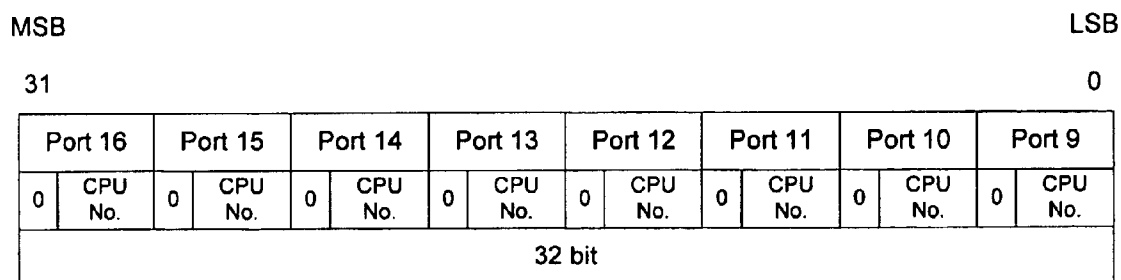


FIG. 18

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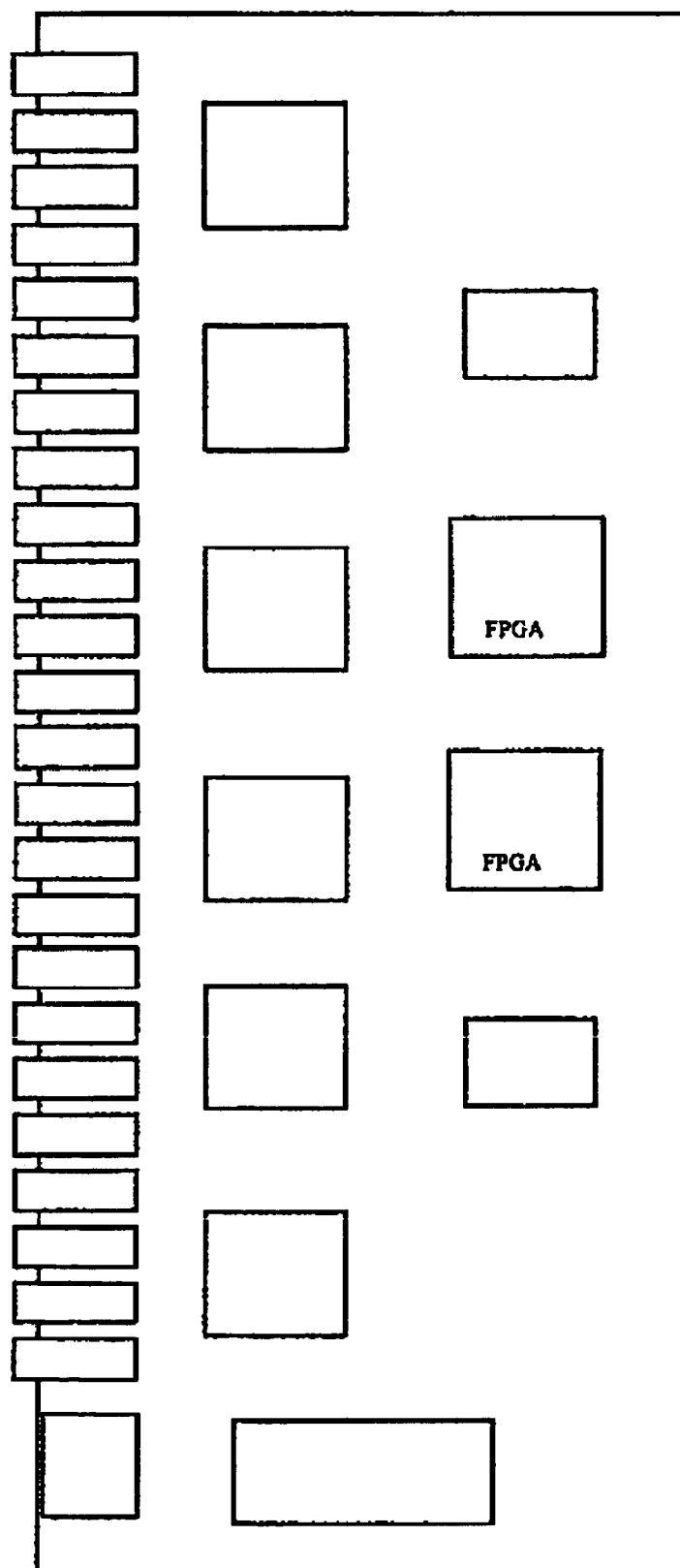


FIG. 19

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TEST APPARATUS AND TEST METHOD FOR TESTING PLURALITY OF DEVICES IN PARALLEL

BACKGROUND OF INVENTION

1. Field of the Invention

The present invention relates to a test apparatus and a test method. More particularly, the present invention relates to a test apparatus and a test method which include a plurality of control apparatuses for testing a plurality of devices under test respectively, and for testing the plurality of devices under test in parallel.

2. Background Art

In a conventional test apparatus, a control apparatus controls a plurality of test modules by providing the plurality of test modules with control data through a control bus, and performs the test of one or a plurality of devices under test connected to the test modules in parallel. For example, such a test apparatus is disclosed in specifications of Japanese patents No. 2,583,055, No. 2,583,056, No. 2,583,057, No. 2,587,940, No. , 2,587,941, and No. 2,627,751.

SUMMARY OF INVENTION

When a complicated logical circuit, such as CPU, is to be tested, there are many test items and it is necessary to test a plurality of devices under test using a different test sequences respectively according to the test result. Therefore, it is preferable to test the plurality of devices under test in parallel and independently. However, in the conventional test apparatus, since one control apparatus tests the plurality of devices under test in parallel, it is necessary to process each of the test sequences sequentially when it tests the plurality of devices under test using different test sequences respectively. Therefore, efficiency of the test is not so high.

Moreover, even if when the test apparatus is constituted for testing the plurality of devices under test with the plurality of control apparatuses, it is difficult to make the various kinds of devices under test, of which the numbers of pins are different from each other, always correspond to the control apparatuses and to test the devices under test when the connections between the plurality of test modules and the plurality of devices under test are fixed.

Therefore, it is an object of the present invention to provide a test apparatus and a test method which can solve the foregoing problem. The above and other objects can be achieved by combinations described in the independent claims. The dependent claims define further advantageous and exemplary combinations of the present invention.

Therefore, according to the first aspect of the present invention, there is provided a test apparatus for testing a plurality of devices under test. The test apparatus includes: a plurality of test modules, connected to either of the plurality of devices under test, for supplying a test signal to the connected device under test; a plurality of control apparatuses for controlling the plurality of test modules, and for testing the plurality of devices under test in parallel; and a connection switching section for switching topology of the plurality of control apparatuses and the plurality of test modules so that the plurality of control apparatuses connect with the plurality of devices under test respectively.

The plurality of the control apparatuses may control the plurality of test modules according to a test result of the plurality of devices under test respectively, and may perform different test sequences to the plurality of devices under test in parallel.

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The connection switching section may switch the topology for the test of the plurality of devices under test by the plurality of control apparatuses based on an instruction of one of the plurality of control apparatuses before the test of the plurality of devices under test by the plurality of control apparatuses.

The connection switching section may include: a serial interface for transmitting a data packet received from the test module to the control apparatus; and an IDLE packet generating section for providing an IDLE packet to fill an empty space in serial data transmitted by the serial interface when the serial interface does not receive the data packet from the test module.

The plurality of control apparatuses may include: a performance judging test executing section for ordering to perform a performance judging test to the device under test for judging performance of the device under test; an operational specification determination section for determining operational specifications of the device under test based on result of the performance judging test; an acceptability judging test executing section for ordering to perform an acceptability judging test to the device under test according to the operational specifications determined by the operational specification determination section; and an acceptability judgment section for judging acceptability of the device under test according to the operational specifications determined by the operational specification determination section based on the result of the acceptability judging test.

According to the second aspect of the present invention, there is provided a test apparatus for testing a plurality of devices under test, including a plurality of control apparatuses for testing the plurality of devices under test in parallel. Each of the plurality of control apparatuses includes: a performance judging test executing section for ordering to perform a performance judging test to the device under test for judging performance of the device under test; an operational specification determination section for determining operational specifications of the device under test based on result of the performance judging test; an acceptability judging test executing section for ordering to perform an acceptability judging test to the device under test according to the operational specifications determined by the operational specification determination section; and an acceptability judgment section for judging acceptability of the device under test according to the operational specifications determined by the operational specification determination section based on the result of the acceptability judging test.

The performance judging test executing section may order to perform the performance judging test to the device under test for judging performance of memory of the device under test. The operational specification determination section may determine memory space, which is one of the operational specifications of the device under test, to be a memory space less than that of an operating part of the memory space when a part of the memory is not operating. The acceptability judging test executing section may order perform the acceptability judging test to the device under test, which is determined as a device including the memory space determined by the operational specification determination section. The acceptability judging section may judge the acceptability of the device under test, which is determined as a device including the memory space determined by the operational specification determination section.

According to the third aspect of the present invention, there is provided a test method for testing a plurality of tested devices in parallel with a plurality of control apparatuses respectively. Each of the plurality of control apparatuses

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tuses includes steps of: ordering to perform a performance judging test to the device under test for judging performance of the device under test; determining operational specifications of the device under test based on result of the performance judging test; ordering to perform an acceptability judging test to the device under test according to the determined operational specifications; and an acceptability judgment step section for judging acceptability of the device under test according to the determined operational specifications based on the result of the acceptability judging test.

The summary of the invention does not necessarily describe all necessary features of the present invention. The present invention may also be a sub-combination of the features described above.

Other aspects and advantages of the invention will be apparent from the following description and the appended claims.

BRIEF DESCRIPTION OF DRAWINGS

FIG. 1 is a block diagram exemplary showing a configuration of a test apparatus 10.

FIG. 2 is a block diagram exemplary showing a configuration of the test apparatus 10.

FIG. 3 is a block diagram exemplary showing a functional configuration of a site control apparatus 130a.

FIG. 4 is a block diagram exemplary showing a hardware configuration of a connection switching section 140.

FIG. 5 is a block diagram exemplary showing a hardware configuration of the connection switching section 140.

FIG. 6 shows an example of a data configuration of a Config register 250.

FIG. 7 shows an example of connection switching setting data.

FIG. 8 shows a write side connection concept chart.

FIG. 9 shows read side connection concept chart.

FIG. 10 shows a Status Register.

FIG. 11 shows a Class Code & Revision ID Register.

FIG. 12 shows a Module ID & Vendor ID Register.

FIG. 13 shows a Bus Number Register.

FIG. 14 shows a FPGA Rev. & Board Rev. Register.

FIG. 15 shows a Port Sense 1 Register.

FIG. 16 shows a Port Enable 1 Register.

FIG. 17 shows Switch Select 1 Register.

FIG. 18 shows Switch Select 2 Register.

FIG. 19 shows a rough location of the main parts.

DETAILED DESCRIPTION

The invention will now be described based on the preferred embodiments, which do not intend to limit the scope of the present invention, but exemplify the invention. All of the features and the combinations thereof described in the embodiment are not necessarily essential to the invention.

FIG. 1 and FIG. 2 show block diagrams exemplary showing configurations of a test apparatus 10 according to embodiments of the present invention. The test apparatus 10 generates a test signal, supplies it to a DUT 100 (Device Under Test), and judges acceptability of the DUT 100 based on whether a result signal, which is output as a result of the DUT 100 being operated based on the test signal, coincides with an expected value. The test apparatus 10 according to the present embodiment is realized by an open architecture, and a module based on the open architecture is utilized as a test module 150 for supplying the test signal to the DUT 100. Then, a connection switching section 140 switches topology of a site control apparatus 130 and the test module 150

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according to the number of pins of the DUT 100, form of wiring of a load module 160, kind of the test module 150, etc. Thereby, in the test apparatus 10, the site control apparatuses 130 connect with the corresponding DUTs 100 one to one, and one of the site control apparatuses 130 tests the corresponding DUT 100. Therefore, the plurality of site control apparatuses 130a-130h test the plurality of DUTs 100s in parallel, and the plurality of site control apparatuses 130a-130h further perform different test sequences according to the performance of the DUTs 100 respectively.

The test apparatus 10 includes a system controller 110, a telecommunication network 120, the site control apparatuses 130a-130h, the connection switching section 140, the test modules 150a-150f, and load boards 160a-160d, and connect with the DUTs 100a-100d.

The system controller 110 receives and stores a test control program, a test program, test data and the like, which is used for the test apparatus 10 to test the DUTs 100a-100d, through a external network etc. The telecommunication network 120 connects the system controller 110 and the site control apparatuses 130a-130h, and relays communication between them.

The site control apparatuses 130a-130h are examples of control apparatuses according to the present invention. The site control apparatuses 130a-130h control a plurality of test modules, and test each of the plurality of DUTs 100 in parallel. Here, the plurality of site control apparatuses 130a-130h control the test of the plurality of DUTs 100 respectively. For example, in FIG. 1, the site control apparatus 130a connects with the test modules 150a-150f connected to the DUT 100a, and controls the test of the DUT 100a. Moreover, in FIG. 2, the site control apparatus 130a connects with the test modules 150a-150b connected to the DUT 100b, and controls the test of the DUT 100a, and the site control apparatus 130b connects with the test modules 150c-150d connected to the DUT 100c, and controls the test of the DUT 100c.

More specifically, the site control apparatuses 130a-130h acquire the test control program from the system controller 110 through the telecommunication network 120 and execute it. Next, based on the test control program, the site control apparatuses 130a-130h acquire the test program and the test data, which are used for the test of the DUTs 100a-100d, from the system controller 110, and store them in the test modules 150a-150f used for the test of the DUTs 100 through the connection switching section 140. Next, the site control apparatus 130a-130h instruct the start of the test based on the test program and the test data to the test modules 150a-150f through the connection switching section 140. Then, the site control apparatuses 130a-130h receive the interruption, which indicates that the test is completed, from the test modules 150a-150f for example, and cause each of the modules to perform the next test based on the test result. That is, the plurality of site control apparatuses 130a-130h control the plurality of test modules 150a-150f according to the test result of the plurality of DUTs 100 respectively, and perform different test sequences to the plurality of DUTs 100 in parallel.

The connection switching section 140 switches the topology of the plurality of site control apparatuses a-h and the plurality of test module 150a-150f so that the plurality of site control apparatuses 130a-130h connect with the plurality of DUTs 100 respectively. That is, each of the plurality of site control apparatuses 130a-130h connects with either of the test modules 150a-150f, which are controlled by the site control apparatuses 130a-130h respectively, so as to relay the communication between them.

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The connection switching section 140 switches the topology of the plurality of site control apparatuses 130a–130h and the plurality of test modules 150a–150f during the test of the plurality of DUTs 100s by the plurality of site control apparatus 130a–130h based on instruction of a site control apparatus 130 among the plurality of site control apparatuses 130a–130h before the test of the plurality of DUTs 100 by the plurality of site control apparatuses 130a–130h. For example, in FIG. 2, the site control apparatus 130a is set up so that it connects with the plurality of test modules 150a–150b, thereby the test of the DUT 100b is performed. Moreover, the site control apparatus 130b is set up so that it connects with the plurality of test modules 150c–150d, thereby the test of the DUT 100c is performed.

The plurality of DUTs 100 are mounted on the load boards 160a–160d, and the plurality of test modules 150a–150f connect with the corresponding terminals of the DUTs 100.

Since a configuration and operation of the site control apparatuses 130a–130h shown in FIG. 2 for testing the DUTs 100a–100d using the plurality of test modules 150a–150f are substantially the same as that of the site control apparatus 130a shown in FIG. 1 for testing the DUT 100a using the plurality of test modules 150a–150f, the configuration and the operation of the site control apparatus 130a shown in FIG. 1 for testing the DUT 100a will be mainly explained hereinafter unless there is an expectation.

The plurality of test modules 150a–150f connect with a part of the plurality of terminals of the DUT 100a respectively, and test the DUT 100a based on the test program and the test data stored in the site control apparatus 130a. During the test of the DUT 100a, the test modules 150a–150f generate the test signal from the test data based on the sequence defined by the test program, and supply the test signal to the terminals of the DUT 100a connected to the test modules 150a–150f respectively. Then, the result signal, which is output as a result of the DUT 100a being operated based on the test signal, is acquired, whereby the result signal is compared with an expected value and the comparison result is stored.

Moreover, the test modules 150a–150f generate the interruption to the site control apparatus 130a when the processing of the test program has been completed, or when an abnormality occurs during the execution of the test program. The interruption is notified to the site control apparatus 130a corresponding to the test modules 150a–150f through the connection switching section 140, and the interrupt processing is performed by the processor of the site control apparatus 130a.

As stated above, the test apparatus 10 is realized by an open architecture, and various kinds of modules which satisfy the standard of the open architecture are utilized. Then, the test apparatus 10 is utilized by inserting the test modules 150a–150f to any connection slots of the connection switching section 140. In this case, a user of the test apparatus 10 etc. changes the topology of the connection switching section 140 through the site control apparatus 130a for example, and connects the plurality of test modules 150a–150f used for the test of the DUTs 100 and either of the site control apparatuses 130a–130h for controlling the test of the DUTs 100. Thereby, the user of the test apparatus 10 connects appropriately the plurality of site control apparatuses 130a–130h and the test modules 150a–150f according to the number of the terminals, arrangement of the terminals, kind of the terminals, kind of the test, etc., of each of the DUTs 100. Then, the user of the test apparatus 10 makes the site control apparatuses 130 correspond to the DUTs 100 one to one, and the plurality of DUTs 100 are

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tested in parallel and independently. Therefore, even when the plurality of DUTs 100 are tested by different test sequences, test duration is shortened by testing the plurality of DUTs 100 in parallel.

FIG. 3 is a block diagram exemplary showing a functional configuration of the site control apparatus 130 according to the present embodiment. Each of the site control apparatuses 130a–130h includes: a performance judging test executing section 170 for ordering the execution of the performance judging test of the DUT 100 for judging the performance of the DUT 100; an operational specification determination section 180 for determining operational specifications of the DUT 100; a test condition storage section 190 for storing kind of the test condition of an acceptability judging test in association with the operational specifications of the DUT 100; an acceptability judging test executing section 200 for ordering the execution of the acceptability judging test to the DUT 100; and an acceptability judging section 205 for judging the acceptability of the DUT 100 according to the operational specifications determined by the operational specification determination section 180.

The performance judging test executing section 170 causes the test module 150 to perform the performance judging test for judging performance of memory of the DUT 100, such as memory space (e.g., cache size) a test frequency, a system bus frequency, permissible voltage, electric power consumption, drive capability to the system bus, etc., as the performance of the DUT 100. And, the operational specification determination section 180 determines the memory space, the test frequency, the system bus frequency, the permissible voltage, the electric power consumption, the drive capability, etc. as the operational specifications of the DUT 100 based on the result of the performance judging test by the performance judging test executing section 170. For example, when a part of the memory of the DUT 100 is not operating, the memory space, which is one of the operational specifications of the DUT 100, is determined to be the memory space less than that of an operating part of the memory of the DUTs 100.

Then, the acceptability judging test executing section 200 selects the test condition of the acceptability judging test from the test condition storage section 190 according to the operational specifications determined by the operational specification determination section 180. Then, the acceptability judging test executing section 200 causes the test module 150 to perform the acceptability judging test according to the operational specifications determined by the operational specification determination section 180. Specifically, the acceptability judging test is performed to the DUT 100, assuming that the DUT 100 is a device including the memory space determined by the operational specification determination section 180 and operating at the test frequency, the system bus frequency, the permissible voltage, the electric power consumption, and/or the drive capability, which are determined by the operational specification determination section 180. Then, the acceptability judging section 205 judges the acceptability of the DUT 100 based on the result of the acceptability judging test by the acceptability judging test executing section 200, assuming that the DUT 100 is a device including the memory space determined by the operational specification determination section 180 and operating at the test frequency, the system bus frequency, the permissible voltage, the electric power consumption, and/or the drive capability, which are determined by the operational specification determination section 180.

According to the site control apparatus 130 of the present embodiment, the operational specifications are determined

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and selected based on the result of the performance test of the DUT 100, the test is performed by the test sequence according to the selected operational specifications, and then it judges whether the conditions according to the selected operational specifications are satisfied. Furthermore, since the plurality of site control apparatuses 130a–130h correspond to the plurality of DUTs 100 one to one, the plurality of site control apparatuses 130a–130h perform the test of the plurality of DUTs 100 using different sequences respectively in parallel, thereby the selection of the operational specifications and the test are performed efficiently.

FIG. 4 is a block diagram exemplary showing the hardware configuration of the connection switching section 140 according to the present embodiment. FIG. 4 shows a portion used for data transfer from the site control apparatus 130 to the test module 150 among the hardware configuration of the connection switching section 140.

The connection switching section 140 includes a plurality of O/E decoders 210a–210h, a plurality of FIFO register memories 220a–220h, a plurality of FIFO controllers 230a–230h, a Config controller 240, a Config register 250, a plurality of multiplexers 260a–260g, and a plurality of O/E decoders 270a–270g.

The plurality of O/E decoders 210a–210h receive the control data, such as write-in command and write-in data or read-out command to/from the record area in the test modules 150a–150g, from the plurality of site control apparatuses 130a–130h respectively, carry out photoelectric conversion of the control data, and supply them to the plurality of FIFO register memories 220a–220h respectively. The plurality of FIFO register memories 220a–220h acquire the control data, of which the photoelectric conversion is performed by the plurality of O/E decoders 210a–210h respectively, and temporarily store them. The plurality of FIFO controllers 230a–230h read the control data from the plurality of FIFO register memories 220a–220h respectively, and supply them to the plurality of multiplexers 260a–260g respectively.

The Config controller 240 acquires setting data including connection switching setting data of the connection switching section 140 among the control data read by the FIFO controller 230a. Then, the Config register 250 stores the connection switching setting data acquired by the Config controller 240, and sets up the plurality of multiplexers 260a–260g. The plurality of multiplexers 260a–260g select either of the control data read by the FIFO controllers 230a–230h based on the connection switching setting data stored in the Config register 250, and supply it to the plurality of O/E decoders 270a–270g respectively. The plurality of O/E decoders 270a–270g carry out current to light transference of the control data selected by the plurality of multiplexers 260a–260g respectively, and transmit them to the test modules 150a–150g respectively.

As described above, when the Config register 250 stores the connection switching setting data supplied from the site control apparatus 130a, the multiplexers 260a–260g are set up, and the site control apparatuses 130a–130h and the test modules 150a–150g are connected so that the plurality of site control apparatuses 130a–130h correspond to the plurality of DUT 100s one to one.

FIG. 5 is a block diagram exemplary showing a hardware configuration of the connection switching section 140 according to the present embodiment. FIG. 5 shows a part of the hardware configuration of the connection switching section 140, the part being used for the transfer of the data, such as a response to the write-in command or read-out data

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in response to the read-out command, from the test module 150 to the site control apparatus 130.

The connection switching section 140 further includes a plurality of FIFO register memories 280a–280g, a plurality of FIFO controllers 290a–290g, a plurality of multiplexers 300a–300h, a plurality of arbiters 310a–310h, and a plurality of IDLE packet generating sections 320a–320h. In addition, the O/E decoders 210a–210h are examples of the serial interface of the present invention, and transmit the data packets received from the test modules 150a–150g to the site control apparatuses 130a–130h.

The plurality of O/E decoders 270a–270g receive the read-out data, which are the data indicating the test result of the DUT 100 and output from the plurality of test modules 150a–150g respectively based on the demand of the plurality of site control apparatuses 130a–130h. Then the plurality of O/E decoders 270a–270g carry out photoelectric conversion of the read-out data and supply them to the plurality of FIFO register memories 280a–280g respectively. The plurality of FIFO register memories 280a–280g acquire the read-out data, of which the photoelectric conversion is carried out by the plurality of O/E decoders 270 respectively, and temporarily store the read-out data. The plurality of FIFO controllers 290a–290g read the read-out data from the plurality of FIFO register memories 280a–280g respectively.

Each of the plurality of FIFO controllers 290a–290g includes a plurality of REQ output terminals for requesting data transfer to the plurality of multiplexers 300a–300h, and outputs a request command (REQ) to the multiplexer 300 which requests the data transfer. Moreover, each of the FIFO controllers 290a–290g includes a GNT input terminal for receiving a response from the plurality of multiplexers 300a–300h in response to the REQ, and receives a grant command (GNT) from the multiplexer 300 which requests the data transfer.

First, the plurality of FIFO controllers 290a–290g supply the REQ to either of arbiters 310a–310h corresponding to the site control apparatus 130 for supplying the read-out data when they supply the read-out data (R_DATA) to either of the site control apparatuses 130a–130h. When the REQ is received from either of the FIFO controllers 290a–290g, the arbiters 310a–310h supply the grant command (GNT) to the FIFO controller 290, which permits the output of the read-out data, among the FIFO controllers 290a–290g based on the connection switching setting data stored in the Config register 250. Then, the FIFO controller 290, which receives the GNT, supplies the R_DATA to the multiplexers 300a–300h.

Based on the control of the arbiters 310a–310h, the plurality of multiplexers 300a–300h select the R_DATA from the FIFO controller 290, to which the arbiters 310a–310h supply the GNT, respectively, and supply them to the plurality of O/E decoders 210a–210h respectively. The plurality of O/E decoders 210a–210h carry out the current to light transference of the R_DATA selected by the plurality of multiplexers 300a–300h respectively, and transmit them to the corresponding control apparatuses 130a–130h respectively.

In case that the plurality of O/E decoders 210a–210h do not receive the data packet from the test modules 150a–150g (i.e., in case that the arbiters 310a–310h have selected neither of the FIFO controllers 290a–290g), the IDLE packet generating sections 320a–320h supply an IDLE packet in the serial data transmitted by the plurality of O/E decoders 210a–210h to fill empty space of the serial data transmitted by the plurality of O/E decoders 210a–210h to

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the test modules 150a–150g. Moreover, the multiplexer 300a acquires the setting data, which the Config controller 240 reads from the Config register 250, and supplies it to the site control apparatus 130a.

As described above, when the arbiters 310a–310h select the FIFO controllers 290a–290g, from which the multiplexers 300a–300h are to acquire the read-out data, based on the connection switching setting data stored in the Config register 250, the site control apparatus 130 acquires the read-out data from the test module 150 which has transmitted the control data.

FIG. 6 shows an example of the data configuration of the Config register 250 according to the present embodiment. The Config register 250 stores the connection switching setting data (Switch Select1–Switch Select8) in association with address (17–1Eh), i.e., the site control apparatus 130 selected by the plurality of multiplexers 260 respectively. For example, the Switch Select 1 stored in address 17h is the connection switching setting data for setting up the 1–8th multiplexers 260, and the Switch Select 2 stored in address 18h is the connection switching setting data for setting up the 9–16th multiplexers 260. The Config register 250 stores the connection switching setting data, of which the number corresponds to the number of the multiplexers 260 of the connection switching section 140.

FIG. 7 shows an example of the connection switching setting data according to the present embodiment. FIG. 7 shows concrete contents of the connection switching setting data (Switch Select 1) 300 shown in FIG. 6.

The Config register 250 stores a number of the site control apparatus 130 (CPU NO.) and validity of the setting (ON/OFF) in association with the ports (Port1–Port8) of the connection switching section 140. The ports (Port1–Port8) of the connection switching section 140 corresponds to the 1–8th multiplexers 260, and the number of the site control apparatus 130 (CPU NO.) indicates the site control apparatus 130 selected by the 1–8th multiplexers 260.

In the present embodiment, although the Config register 250 stores the validity of the setup of the connection switching of the connection switching section 140, the same function as the present embodiment is realized by another means, such as the site control apparatus 130 controlling the validity of the setup.

By the data configuration of the Config register 250 described above, it is realizable for the plurality of site control apparatus 130 to test the plurality of DUTs 100 in parallel, by switching the site control apparatus 130 selected by the plurality of multiplexers 260, and by connecting the site control apparatus 130 and the DUT 100 so that they correspond to each other one to one.

Next, an example of the specification of the connection switching section 140 according to the present embodiment will be shown.

An OPENSTARBus Switch Control design specification is presented as an example. This SWITCH board can select and switch an arbitrary high-speed optical serial bus connection of OPENSTARBus of 8 CPUs and 16 Modules. This board has the function of forwarding the WRITE DATA from CPU to the port of the module arbitrarily selected. And it forwards the READ DATA from the module to the selected CPU.

A functional block diagram is shown in FIGS. 8–9. As can be seen in FIG. 8, WRITE DATA from the CPU is forwarded to the module side ports selected by configuration register. As can be seen in FIG. 9, READ DATA from the module side is stored to the FIFOs once. Then it is forwarded to CPU side selected by the configuration register and arbitrated

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between buses. The timing between IDLE packet and DATA packet and the timing in the bus are adjusted.

With respect to the Bus Switch setting procedure, the Configuration command can change the setting of the switches. The following steps are the procedure to change the settings. This settings can only be changed from CPU1. So, only CPU1 must set the settings. To change the bus, it must set the state to continue to generate the IDLE packet.

- (1) Prohibit to write the data to FIFO in this board.
- (2) Switch the setting of Bus Switch to CPU “1” for Bus configuration.
- (3) Waiting at time (Wait at time that Bus changes.)
- (4) Remove the Write prohibition to FIFO.
- (5) Set some configuration, then the DATA forwarding and other settings to each port.
- (6) Prohibit to writing the data to FIFO.
- (7) Switch the setting of Bus Switch.
- (8) Waiting at time (Wait at time that Bus changes.) (9) Remove the Write prohibition of FIFO.
- (10) It can use as the measurement etc.

* Wait time is the fixed time (** ns) by the software
The configuration register map is included below as table 1.

TABLE 1

Configuration Register Map						
Name	Address	R/W	Bit31 MSB- bit24	Bit23- bit16	Bit15- bit8	Bit8- bit0 LSB
Reserve	00 h				Reserve	
Status	01 h	R/W		Status	Reserve	
Class	02 h	R		Class Code	Command(Reset etc.)	
Code & Revision						Revision ID
Reserve	03 h	R	Reserve	Header Type	Reserve	
Base Address 0	04 h	R/W		Base Address 0		
Base Address 1	05 h	R/W		Base Address 1		
Base Address 2	06 h	R/W		Base Address 2		
Reserve	07 h				Reserve	
Reserve	08 h				Reserve	
Reserve	09 h				Reserve	
Reserve	0A h				Reserve	
Module ID & Vendor ID	0B h	R	Module ID		Vendor ID	
Reserve	0C h				Reserve	
New	0D h	R		Reserve		New
Capability Pointer						Capability Pointer
Bus Number	0E h	R/W		Reserve		Bus Number
Revision	0F h	R		FPGA Rev		Board Rev
Module Info capability	10 h	R	Reserve		Next Capability Pointer	Capability ID
Port Sense 1	11 h	R			Port Sense 1	
Port Sense 2	12 h	R			Port Sense 2	
Port Enable 1	13 h	R/W			Port Enable 1	
Port Enable 2	14 h	R			Port Enable 2	
Port size & control	15 h	R	Reserve	Port Size for Site CPU	Port Size for Module	Port Control
Bridge	16 h	R/W	Reserve		Next	Capability

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TABLE 1-continued

Configuration Register Map						
Name	Address	R/W	Bit31 MSB- bit24	Bit23- bit16	Bit15- bit8	Bit8- bit0 LSB
Info capability					Capability Pointer	ID
Switch Select 1	17 h	R/W		Switch Select 1		
Switch Select 2	18 h	R/W		Switch Select 2		
Switch Select 3	19 h	R/W		Switch Select 3		
Switch Select 4	1A h	R/W		Switch Select 4		
Switch Select 5	1B h	R/W		Switch Select 5		
Switch Select 6	1C h	R/W		Switch Select 6		
Switch Select 7	1D h	R/W		Switch Select 7		
Switch Select 8	1E h	R/W		Switch Select 8		
Switch Info	1F h	R	Reserve		Next Capability Pointer	Capability ID
Reserve	20 h~ FF h				Reserve	

Configuration Registers will be set forth with more detail below.

As shown in FIG. 10, Status: Address: 01h. Non Reset Register: Reset Value: None.

As shown in FIG. 11, Class Code & Revision ID: Address: 02h. Read Only Register. Non Reset Register: Reset Value: None.

Header Type Register: Address: 03h.

Base Address Register 0~2: Address: 04h~06h . No Register in GBSC, this Register does not exist.

As shown in FIG. 12, Module ID & Vendor ID Register: Address: 0Bh. Read Only Register. Non Reset Register: Reset Value: None.

New Capability Pointer Register: Address: 0Dh. Read Only Register. Non Reset Register: Reset Value: None.

As shown in FIG. 13, Bus Number Register: Address: 0Eh. Read/Write Register. Non Reset Register: Reset Value: ffh. An initial value is set to ffh, and written with CPU at configuration.

As shown in FIG. 14, FPGA Rev. & Board Rev. Register: Address: 0Fh. Read Only Register. Non Reset Register: Reset Value: None. FPGA Rev: FPGA Revision Number.

Module Info Capability Register: Address: 10h . Read Only Register. Non Reset Register: Reset Value:

As shown in FIG. 15, Port Sense 1 Register: Address: 11h . Read Only Register. Non Reset Register: Reset Value: none. 1: Optical Cable ON. 0: Optical Cable OFF.

Port Sense 2 Register: Address: 12h . No Register in GBSC, the register does not exist.

As shown in FIG. 16, Port Enable 1 Register: Address 13h . Read/Write Register. Power ON Reset Register: Reset Value: 00000000h . Port Enable on P0~P31: Module side (Port 0~P0. Port 1~P1 . . . , Port 15~P15, P16~P31=not exist). 1: Enable Assume that the port can be used, and throw packets other than IDLE. 0: Disable Assume the port not to able to be used, and throw only the packet of IDLE. It is always Disable if Port Sense is 0(Light is off).

Port Enable 2 Register: Address 14h . No Register in GBSC, the register does not exist.

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Port Size & Control Register: Address 15h . No Register in GBSC, the register does not exist.

Bridge Info Capability Register: Address: 16h . As shown in FIG. 17, Switch Select 1 Register: Address 17h . Read/Write Register. Power ON Reset Register: Reset Value: 00000000h . Set the value of CPU No. A site CPU is connected to each Port 1~8 of the module side. Site CPU No. 1: 000. Site CPU No. 2: 001. Site CPU No. 3: 010. Site CPU No. 4: 011. Site CPU No. 5: 100. Site CPU No. 6: 101. Site CPU No. 7: 110. Site CPU No. 8: 111. Selection of Port Enable(ON) 1: When there is a connection in Port. 0: When there is no connection in Port (There is no Module.).

As shown in FIG. 18, Switch Select 2 Register: Address 18h . Read/Write Register. Power ON Reset Register: Reset Value: 00000000h . Set the value of CPU No. The Site CPU is connected to Port 9~16. Site CPU No. 1: 000. Site CPU No. 2: 001. Site CPU No. 3: 010. Site CPU No. 4: 011. Site CPU No. 5: 100. Site CPU No. 6: 101. Site CPU No. 7: 110. Site CPU No. 8: 111. Selection of Port Enable(ON) 1: When there is a connection in Port. 0: When there is no connection in Port (There is no Module.).

Switch Select 3~4 Register: Address: 19h~1Eh. No Register in GBSC, the Register does not exist.

Switch Info Capability Register: Address: 1Fh.

Printed wiring board specification: Outside Dimension: 480 mm×150 mm, board thickness: 2.7 mm. Layer composition: 12 layers. Power supply 3.3V, 1.8V. Main Parts:

Optical Module: Device which converts electric signal of 1.0625 GHz and 1 bit serial from light signal and light signal to 1.0625 GHz 1 bit serial electric signal. Connector (Duplex-LC) for the optical fiber has adhered to this module, too.

SERDES: The device to convert 106.25 MHz 10 bits parallel signals to 1.0625 GHz 1 bit serial signal or convert 1.0625 GHz 1 bit serial signal to 106.25 MHz 10 bits parallel signals.

FPGA: Contain 8B/10B Encoder, Decoder Core.

Power supply warning monitor: There are the monitor circuits to check the abnormality (low voltage) of the power supply and blowing of the fuse. It sends the signal to and notifies the monitor board through the connector.

Power consumption.

Signal Name: OpticalSignal: The I/O signal of Optical signal (LC Connector) is shown as follows. Refer to FC-PI 100-M5-SN-I and FC-PI-100_M6_SN-I for details. IN/OUT: 850 nm VCSEL.

Power & Fail: 1: 3.3V 2: GND 3: Fail 4: NC.

FPGA JTAG: 1: TCK 2: GND 3: TDO 4: 3.3V 5: TMS 6: GND 7: NC 8: NC 9: TDI 10: GND.

ROM JTAG: 1: TCK 2: GND 3: TDO 4: 3.3V 5: TMS 6: GND 7: NC 8: NC 9: TDI 10: GND.

FIG. 19 shows a rough location of the main parts.

Timing specification: Refer to the FPGA design specifications for this board.

FPGA: Circuit: Refer to the FPGA design specifications for the circuit etc. of FPGA. Pin Assignment: Refer to the FPGA design specifications for the circuit etc. of FPGA.

Although the present invention has been described by way of an exemplary embodiment, it should be understood that those skilled in the art might make many changes and substitutions without departing from the spirit and the scope of the present invention. It is obvious from the definition of the appended claims that embodiments with such modifications also belong to the scope of the present invention.

As described above, according to the present invention, the test apparatus and the test method for testing a plurality of DUTs in parallel are realizable.

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What is claimed is:

1. A test apparatus for testing a plurality of devices under test having different performances, comprising:
 - a plurality of test modules, connected to either of the plurality of devices under test having different performances, for supplying a test signal to the connected device under test;
 - a plurality of control apparatuses for controlling said plurality of test modules, and for testing the plurality of devices under test having different performances in parallel; and
 - a connection switching section for switching topology of said plurality of control apparatuses and said plurality of test modules so that said plurality of control apparatuses connect with the plurality of devices under test having different performances respectively.
2. The test apparatus as claimed in claim 1, wherein the plurality of said control apparatuses control said plurality of test modules according to a test result of the plurality of devices under test having different performances respectively, and perform different test sequences to the plurality of devices under test having different performances in parallel.
3. The test apparatus as claimed in claim 1, wherein said connection switching section switches the topology for the test of the plurality of devices under test having different performances by said plurality of control apparatuses based on an instruction of one of said plurality of control apparatuses before the test of the plurality of devices under test having different performances by said plurality of control apparatuses.
4. The test apparatus as claimed in claim 1, wherein said connection switching section comprises:
 - a serial interface for transmitting a data packet received from said test module to said control apparatus; and
 - an IDLE packet generating section for providing an IDLE packet to fill an empty space in serial data transmitted by said serial interface when said serial interface does not receive the data packet from said test module.
5. The test apparatus as claimed in claim 1, wherein each of the plurality of control apparatuses comprises:
 - a performance judging test executing section for ordering to perform a performance judging test to the device under test for judging performance of the device under test;
 - an operational specification determination section for determining operational specifications of the device under test based on result of the performance judging test;
 - an acceptability judging test executing section for ordering to perform an acceptability judging test to the device under test according to the operational specifications determined by said operational specification determination section; and
 - an acceptability judgment section for judging acceptability of the device under test according to the operational specifications determined by said operational specification determination section based on the result of the acceptability judging test.
6. A test apparatus for testing a plurality of devices under test having different performances, comprising a plurality of control apparatuses for testing the plurality of devices under

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test having different performances in parallel, wherein each of said plurality of control apparatuses comprises:

- a performance judging test executing section for ordering to perform a performance judging test to the device under test for judging performance of the device under test;
 - an operational specification determination section for determining operational specifications of the device under test based on result of the performance judging test;
 - an acceptability judging test executing section for ordering to perform an acceptability judging test to the device under test according to the operational specifications determined by said operational specification determination section and
 - an acceptability judgment section for judging acceptability of the device under test according to the operational specifications determined by said operational specification determination section based on the result of the acceptability judging test.
7. The test apparatus as claimed in claim 6, wherein said performance judging test executing section orders to perform the performance judging test to the device under test for judging performance of memory of the device under test,
- said operational specification determination section determined memory space, which is one of the operational specifications of the device under test, to be a memory space less than that of an operating part of the memory space when a part of the memory is not operating,
- said acceptability judging test executing section orders to perform the acceptability judging test to the device under test, which is determined as a device including the memory space determined by said operational specification determination section, and
- said acceptability judging section judges the acceptability of the device under test, which is determined as a device including the memory space determined by said operational specification determination section.
8. A test method for testing a plurality of tested devices having different performances in parallel with a plurality of control apparatuses respectively, wherein each of the plurality of control apparatuses comprises the steps of:
- ordering to perform a performance judging test to the device under test having different performances from each other for judging performance of the device under test;
 - determining operational specifications for the respective device under test having different performances from each other of the device under test based on result of the performance judging test;
 - ordering to perform an acceptability judging test to each of the device under test according to the determined operational specifications; and
 - an acceptability judgment step section for judging acceptability of each of the device under test according to the determined operational specifications based on the result of the acceptability judging test.

* * * * *